

L-Band, GaN/SiC, RF Power Transistor

1.2 - 1.4 GHz | 80 W typ | 60% Efficiency typ | 19dB Gain typ | 50 V | 300µs Pulse Length, 10% Duty Cycle

IGN1214M60 and IGN1214M60S are high power GaN-on-SiC RF power transistors that have been designed to suit the unique needs of modern radar systems. They supply a minimum of 60 W of peak output power, with typically >19 dB of gain and 60% efficiency. They operate from a 50 V supply voltage. For optimal thermal efficiency, the transistors are housed in a metal-based package with an epoxy-sealed ceramic lid.

FEATURES

- GaN on SiC HEMT Technology
- Output Power >60 W
- Pre-matched Input and Output Impedance
- High Efficiency - typically 60%
- 100% RF Tested Under 300µs, 10% duty cycle pulse conditions
- RoHS and REACH Compliant
- Full non-linear electrothermal model available, please contact the factory

APPLICATIONS

- L-band Radar Systems

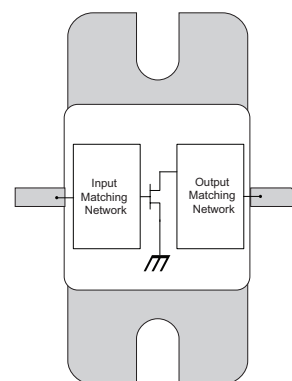


Table 1. RF Electrical Characteristics (Case temperature = 30 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
RF Output Power	$P_{OUT, RF}$	60	80	100	W	$P_{IN} = 0.8W$ $f = 1.2, 1.3, 1.4 \text{ GHz}$ 300µs pulse length 10% duty cycle pulse conditions $V_{DS} = 50V, I_{DS} = 50mA$
Gain	G	18.0	19.0	21.0	dB	
Drain Efficiency	η	50	60	75	%	
Pulse Droop	D	-0.4	-0.2	+0.2	dB	
Input Return Loss	IRL	7	12	18	dB	
Load Mismatch Stability	VSWR-S	2:1				
VSWR Withstand	VSWR-LMT	3:1				

Note: Consult Integra Technologies Application Note 001 for information on how RF output power and pulse droop are measured.

Table 2. Absolute Maximum Ratings (Not Simultaneous)

Parameter	Symbol	Value	Units	Test Conditions
DC Drain-Source Voltage	V_{DS}	120	V	25 °C
DC Gate-Source Voltage	V_{GS}	-8 to +1	V	25 °C
DC Drain Current	I_D	6	A	25 °C
DC Gate Current	I_G	6	mA	25 °C
RF Input Power	$P_{RF,IN}$	1.0	W	25 °C
Operating Channel Temperature	T_{CH}	-55 to +225	°C	
Storage Temperature	T_{STG}	-55 to +150	°C	
Soldering Temperature	T_{SOLDER}	260 for 60s	°C	

Note: Operation outside the limits given in this table may cause permanent damage to the transistor

Table 3. DC Electrical Characteristics (Case temperature = 25 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Gate Pinch-Off Voltage	V_P	-5.0			V	$V_{DS} = 50V, I_{DS} = 1mA$
Quiescent Gate Voltage	V_Q		-2.5		V	$V_{DS} = 50V, I_{DS} = 50mA$

Table 4. Test Fixture Circuit Impedances (Case temperature = 25 °C unless otherwise stated)

Frequency (GHz)	Z_{IF}	Z_{OF}	Units	Test Conditions
1.2	2.5 - j 4.3	15.5 - j 12.2	Ω	$P_{OUT} = 60W$ 300 μs pulse length 10% duty cycle $V_{DS} = 50V, I_{DS} = 50mA$
1.3	2.6 - j 3.3	14.7 - j 10.6	Ω	
1.4	2.8 - j 2.3	14.1 - j 9.0	Ω	

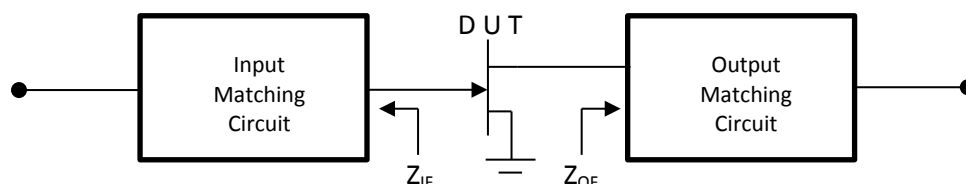
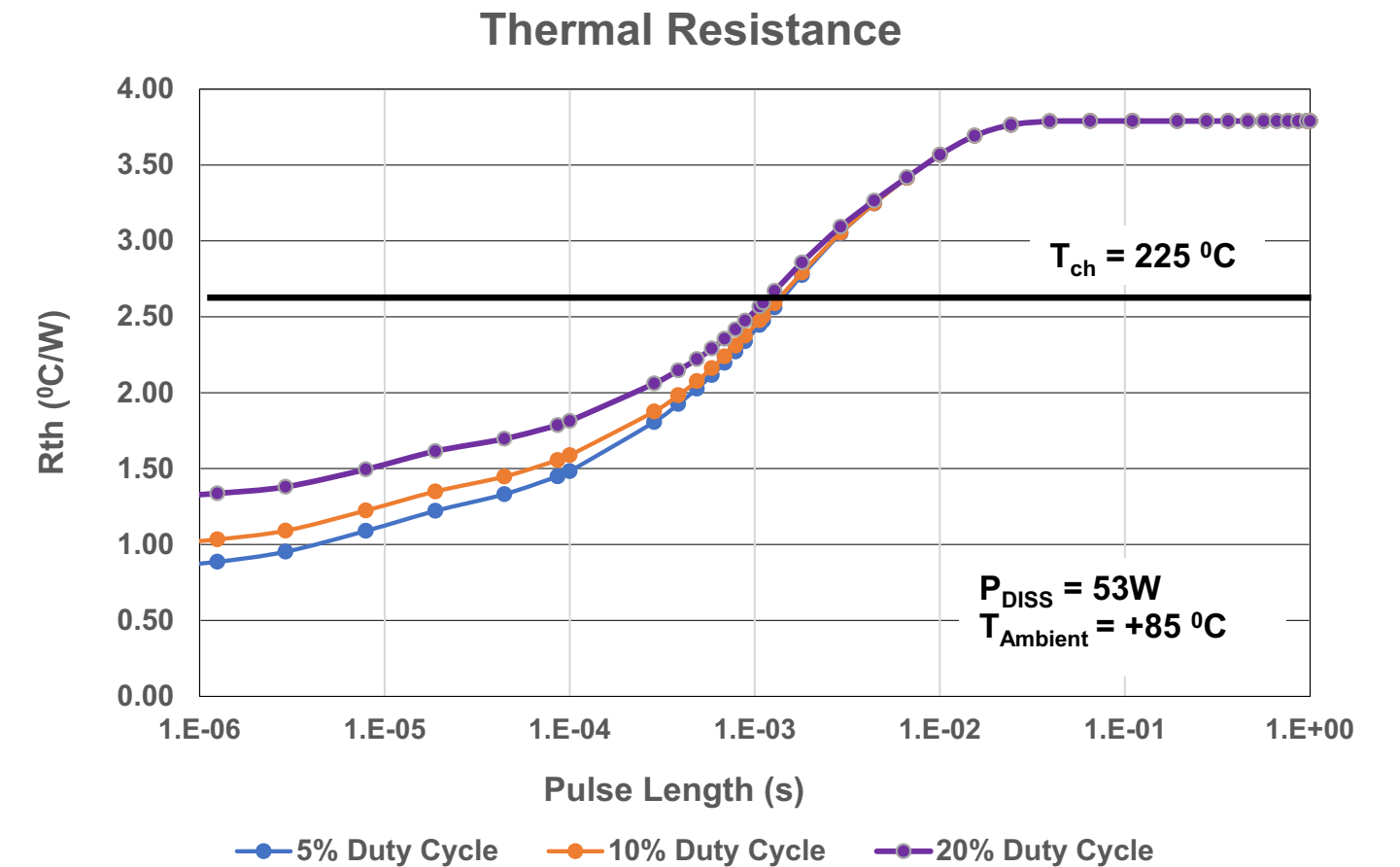


Table 5. Thermal Resistance (Case temperature = 85 °C unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Peak Thermal Resistance, Channel to Case	R_{TH}		2.0		°C/W	$P_{DISS} = 53.3W$ 300µs pulse length 10% duty cycle $V_{DS} = 50V$



TYPICAL RF PERFORMANCE

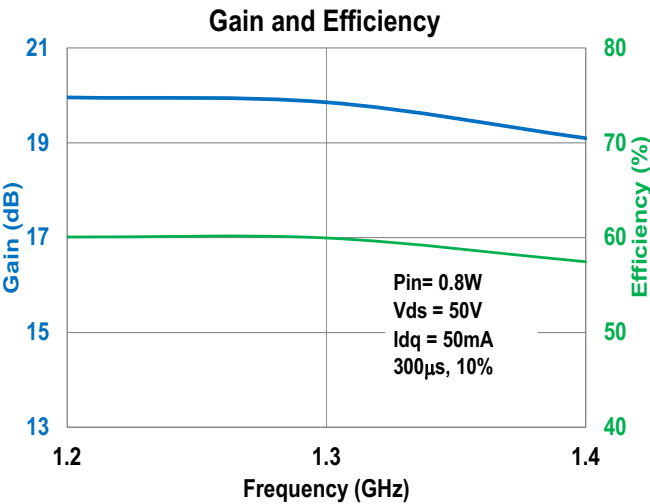


Figure 1

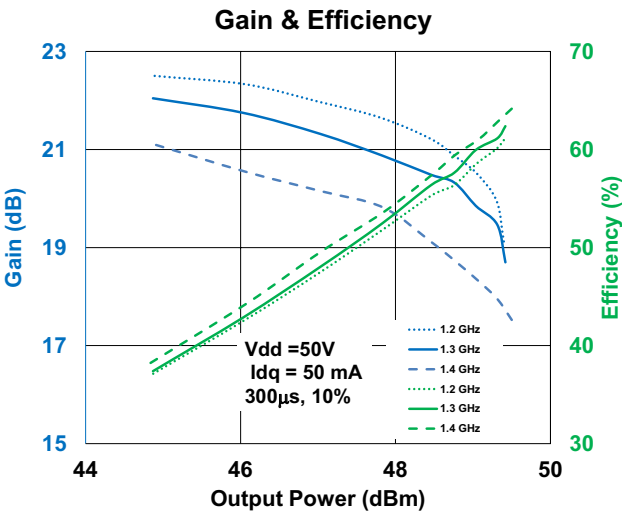


Figure 2

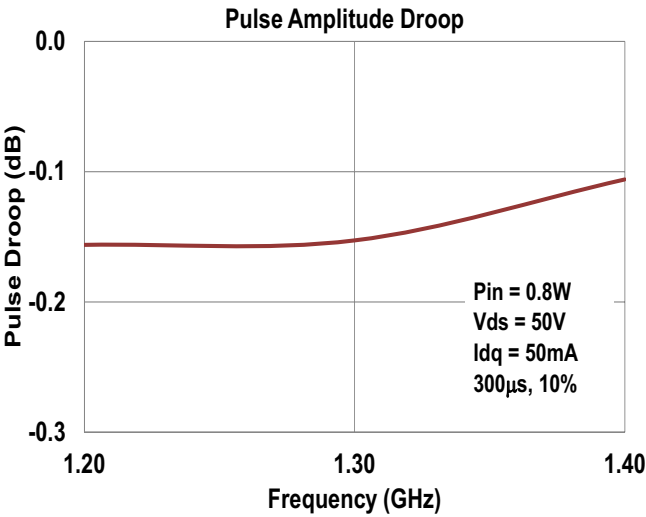


Figure 3

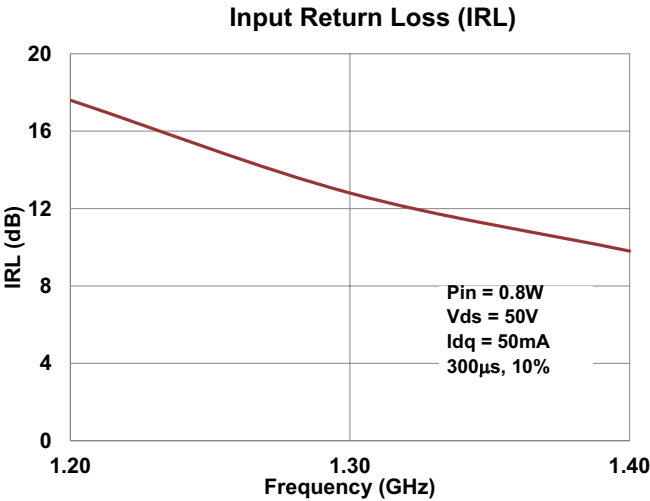
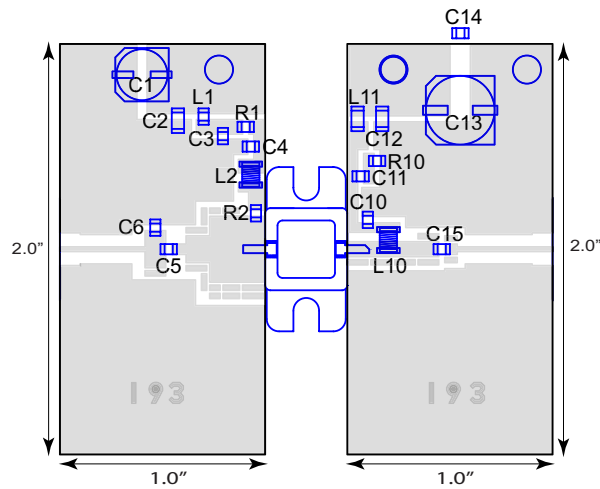


Figure 4

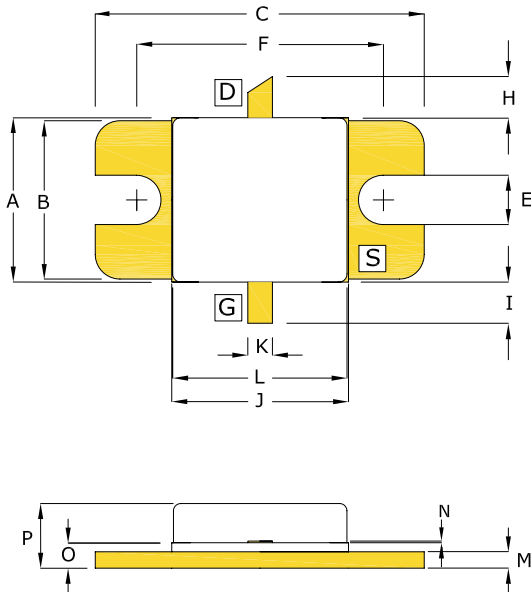
TEST FIXTURE



Bill of Materials for IGN1214M60 Test Fixture

Designator	Description	Quantity
C1	CAP 47 μ F, 25V, Electrolytic	1
C2, C12	CAP 1 μ F, 1206, 100V	2
C3, C11	CAP 0.1 μ F, 0805, 100V	2
C4, C10	CAP 33pF	2
C5	CAP 33pF Edge Mount	2
C6	CAP 1.5pF Edge Mount	1
C13	CAP 68 μ F, 63V, Electrolytic	1
C14	CAP 4700 μ F, 63V, Electrolytic	1
L1	IND FB 120 OHM, 0805, 5A	1
L2, L10	IND 22nH	2
L11	IND FB 33 OHM, 1206, 6A	1
R1, R10	RES 5.1 OHM, 0805	2
R2	RES 15 OHM, 0805	1
PC Board Type	ROGERS RT6010.2, 25mil, 1/1oz. Copper	2

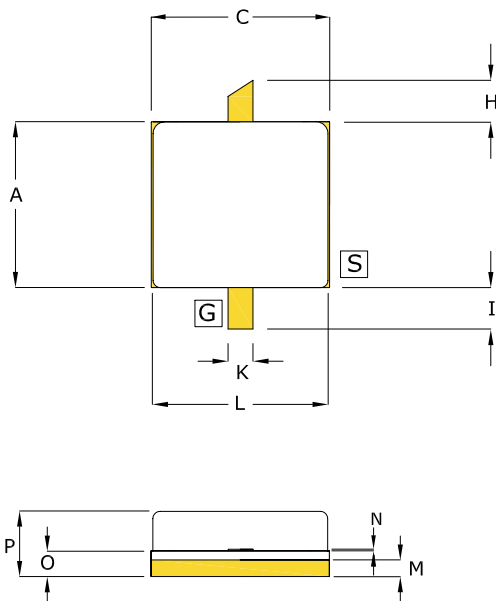
PACKAGE PL44A1



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.395	0.405	10.03	10.29
B	0.380	0.390	9.65	9.91
C	0.795	0.805	20.19	20.45
E	0.115	0.125	2.92	3.18
F	0.595	0.605	15.11	15.37
H	0.090	0.110	2.29	2.79
I	0.090	0.110	2.29	2.79
J	0.425	0.435	10.80	11.05
K	0.055	0.065	1.40	1.65
L	0.420	0.428	10.67	10.87
M	0.035	0.045	0.89	1.14
N	0.004	0.007	0.10	0.18
P	0.053	0.067	1.35	1.70

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

BOLT-DOWN FLANGE OPTION
IGN1214M60



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.393	0.408	9.97	10.35
B	--	--	--	--
C	0.423	0.438	10.73	11.11
E	--	--	--	--
F	--	--	--	--
H	0.090	0.110	2.29	2.79
I	0.090	0.110	2.29	2.79
J	--	--	--	--
K	0.055	0.065	1.40	1.65
L	0.420	0.428	10.67	10.87
M	0.035	0.045	0.89	1.14
N	0.004	0.007	0.10	0.18
P	0.053	0.067	1.35	1.70

PIN SCHEDULE	
D	DRAIN
S	SOURCE
G	GATE

EARLESS FLANGE OPTION
IGN1214M60S

ESD & MSL Rating

Parameter	Rating	Standard
ESD Human Body Model (HBM)	TBD	ESDA/JEDEC JS-001-2012
ESD Charged Device Model (CDM)	TBD	JEDEC JESD22-C101F
Moisture Sensitivity Level (MSL)	Unlimited Shelf Life	IPC/JEDEC J-STD-020

RoHS Compliance

Integra Technologies, Inc declares that its GaN and LDMOS Transistor Products comply with EU Directive 2011/65/EU on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863/EU.

REACH Compliance

Integra Technologies supports EU Regulation number 1907/2006 concerning the Registration, Evaluation, Authorization, and Restriction of Chemicals (REACH) as these apply to Integra semiconductor products, development tools, and shipping packaging.

In support of the REACH regulation, Integra will:

- Inform customers and recipients of Integra product if they contain any substances that are of very high concern (SVHC) per the European Chemical Agency (ECHA) website.
- Notify ECHA if any Integra product that contains any SVHCs which exceed guidelines for REACH chemicals by weight per part number and for total content weight per year for all products produced in or imported to the European market.
- Cease shipments of product containing REACH Annex XIV substances until authorization has been obtained.
- Cease shipment of product containing REACH Annex XVII chemicals when restrictions apply.

Integra has evaluated its materials, BOMs, and product specifications and product and has determined that this transistor conforms to all REACH and SVHC regulations and guidelines. Integra has implemented actions and control programs that will assure continued compliance.

Disclaimer

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DEFINITIONS:

DATA SHEET STATUS

Advanced Specification - This data sheet contains Advanced specifications.

Preliminary Specification - This data sheet contains specifications based on preliminary measurements and data.

Final Specification - This data sheet contains final product specifications.

MAXIMUM RATINGS Stress above one or more of the maximum ratings may cause permanent damage to the device. These are maximum ratings only operation of the device at these or at any other conditions above those given in the characteristics sections of the specification is not implied. Exposure to maximum values for extended periods of time may affect device reliability.